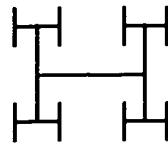


FIG. 9

**TITLE: TECHNIQUE TO SIMULTANEOUSLY DISTRIBUTE
CLOCK SIGNALS AND DATA ON INTEGRATED CIRCUITS,
INTERPOSERS, AND CIRCUIT BOARDS**

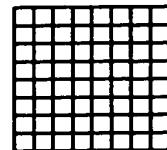
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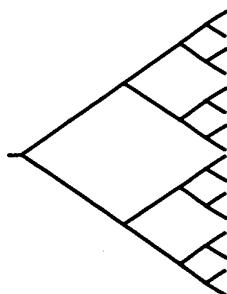
"H" - TREE

**Fig. 1A
(PRIOR ART)**



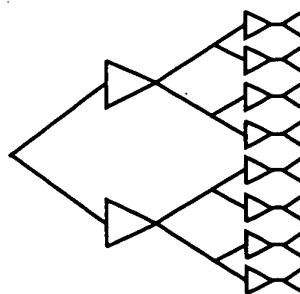
GRID

**Fig. 1B
(PRIOR ART)**



BALANCED TREE

**Fig. 1C
(PRIOR ART)**



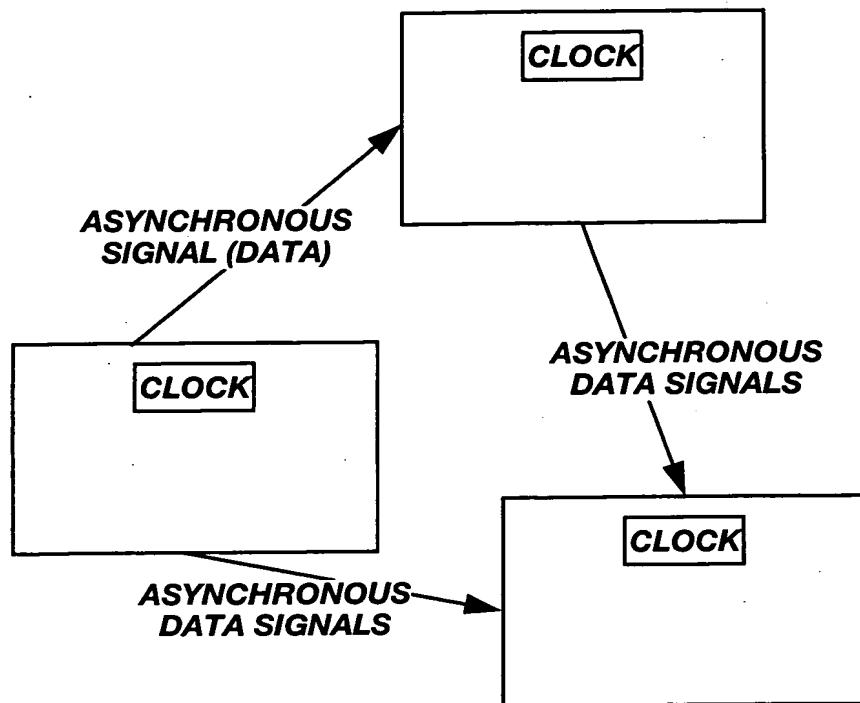
BALANCED TREE WITH BUFFERS

**Fig. 1D
(PRIOR ART)**

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***Fig. 2
(PRIOR ART)***

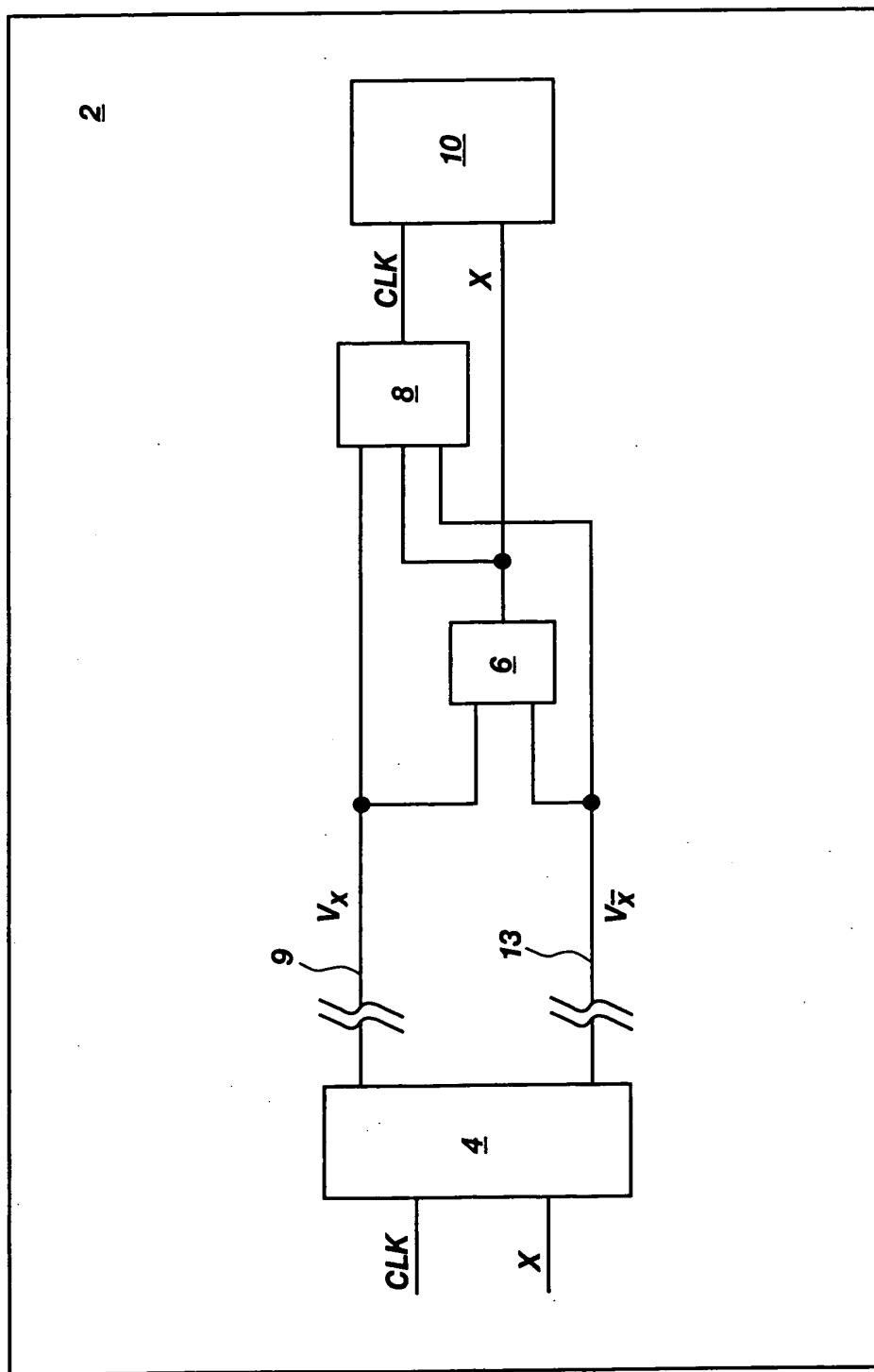


Fig. 3

**TITLE: TECHNIQUE TO SIMULTANEOUSLY DISTRIBUTE
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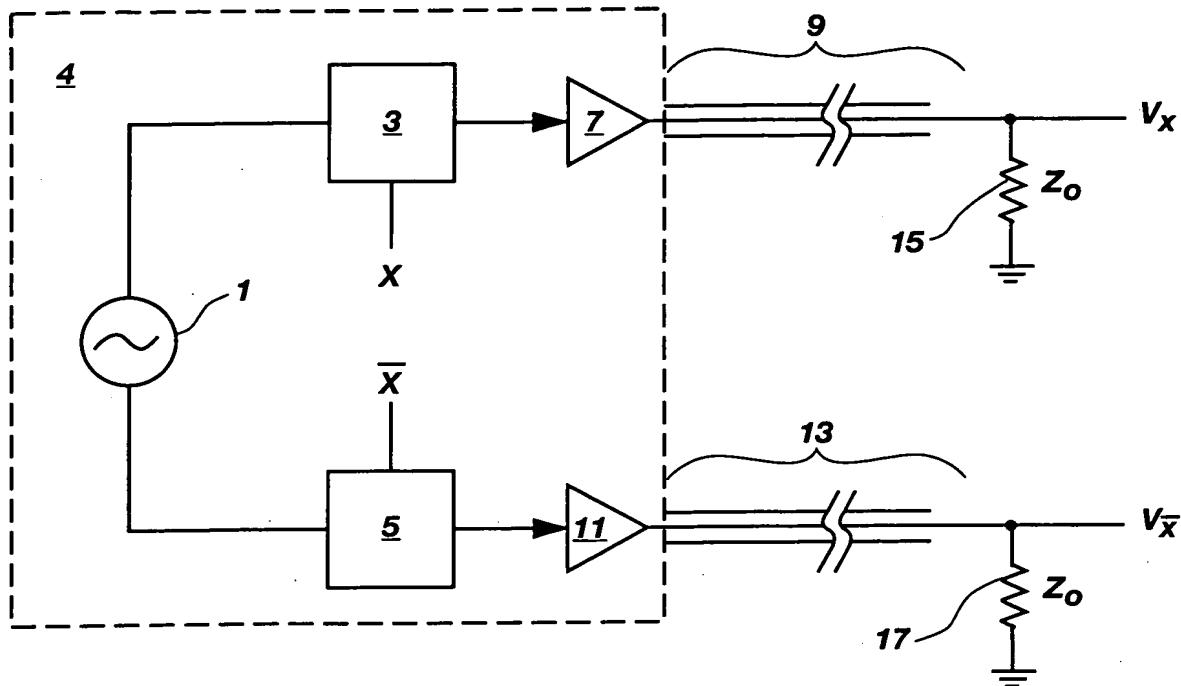


Fig. 4

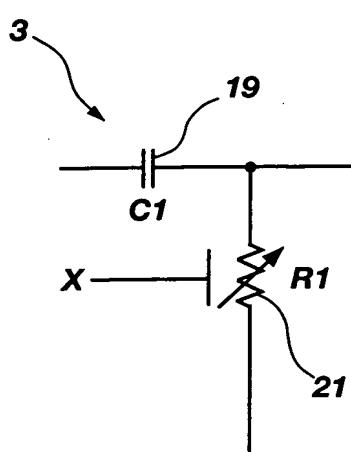


Fig. 5

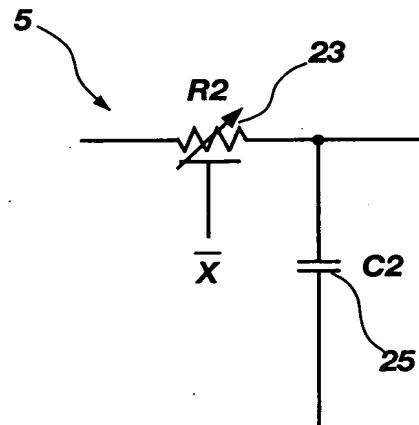


Fig. 6

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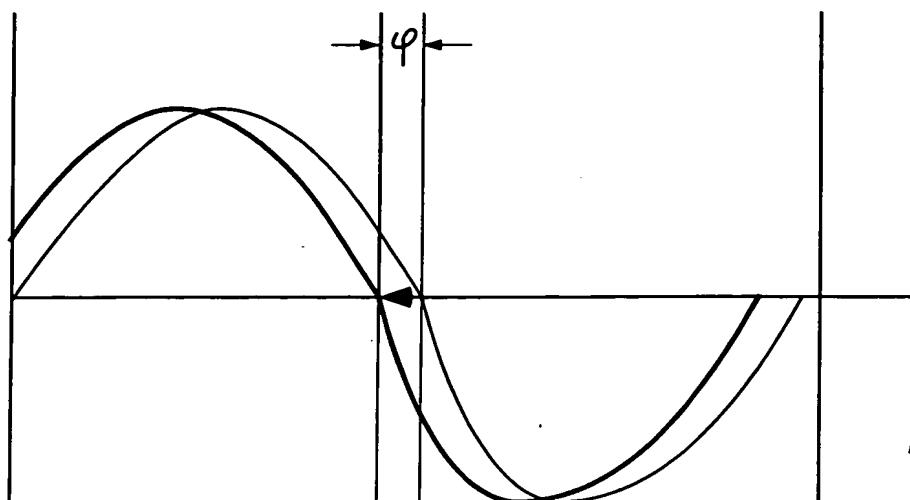


Fig. 7A

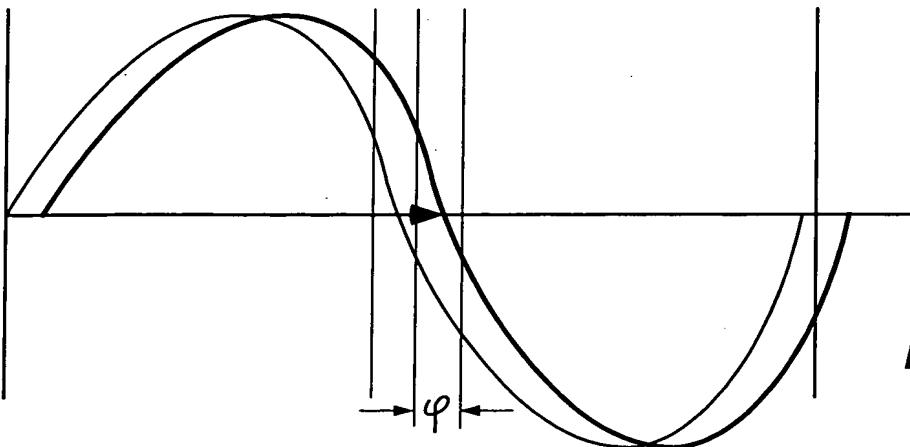


Fig. 7B

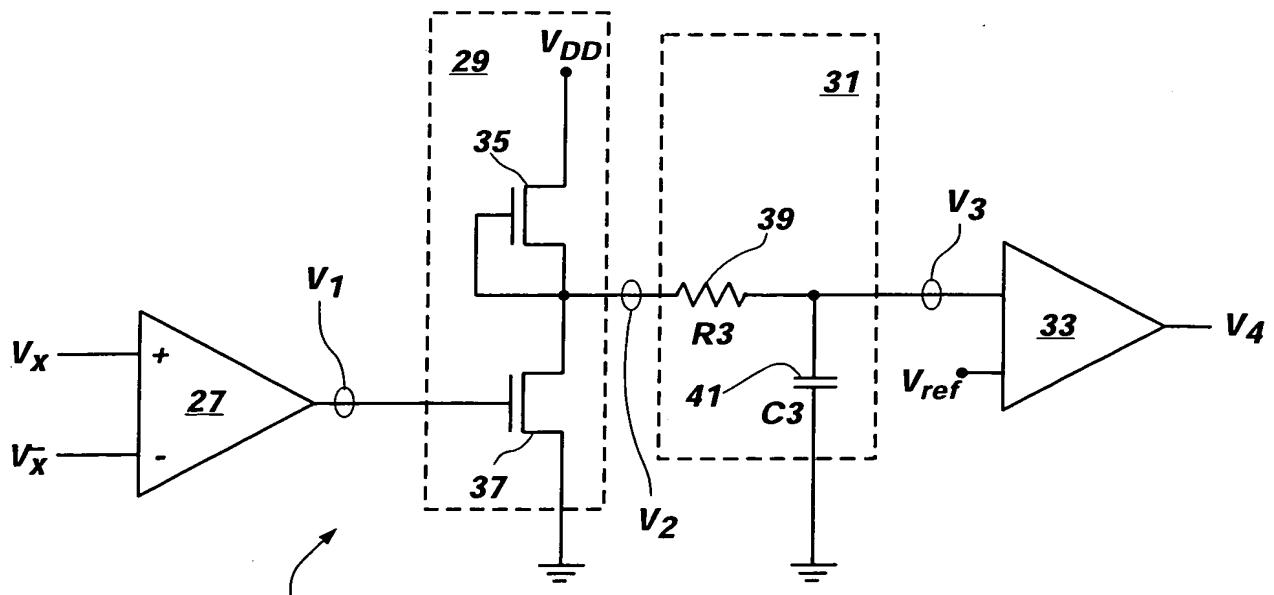


Fig. 8

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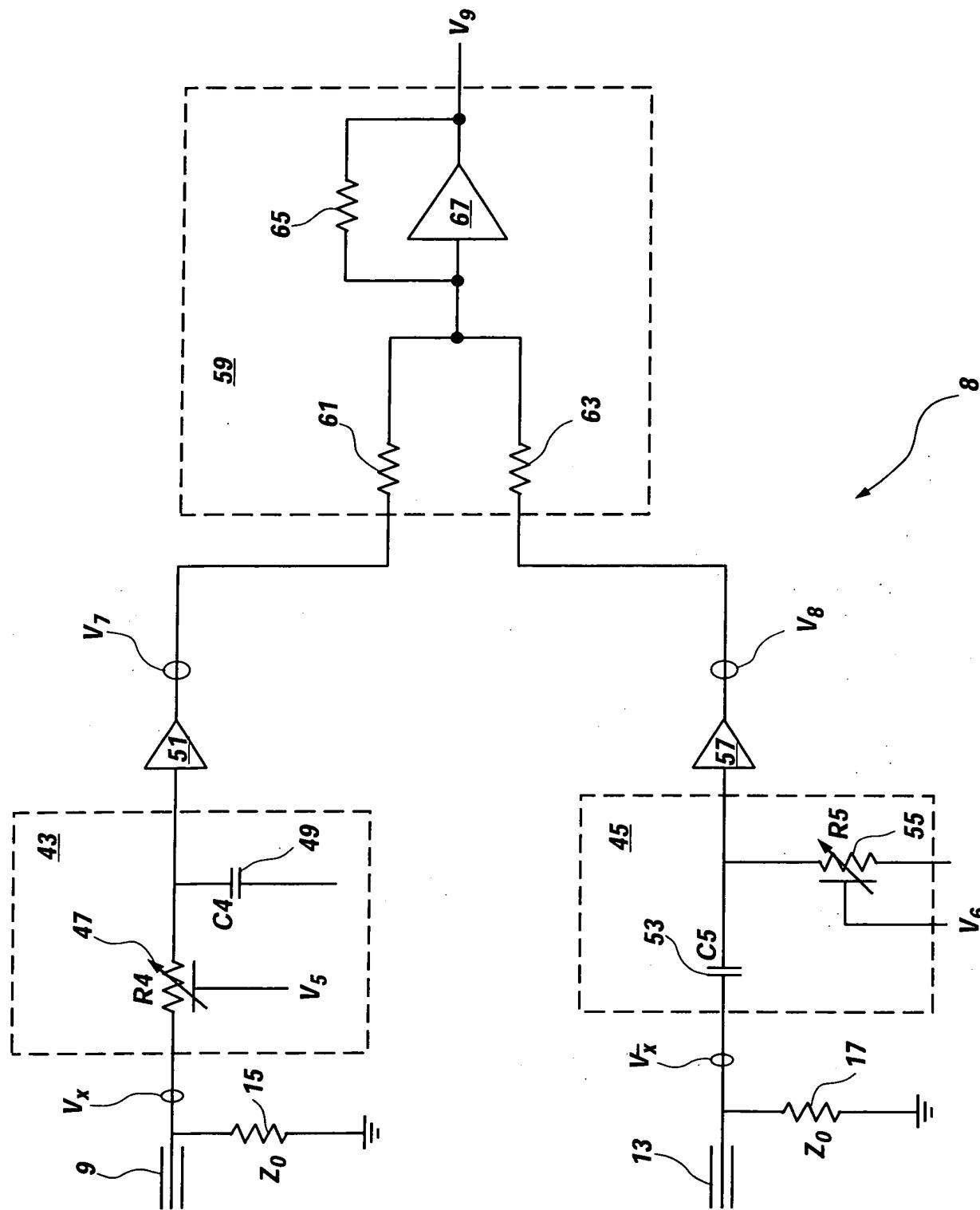


Fig. 9